REMARKS

Applicants respectfully request further examination and reconsideration in view of the instant response. Claims 1-4, 7, 9-12, 14, 16-17, 20-21, and 23 have been amended herein. Claims 1-23 remain pending in the case. No new matter has been added as a result of these amendments.

CLAIM REJECTIONS
35 U.S.C. §112

Claims 2-4, 10-12, and 20-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants have amended Claims 2-4, 10-12, and 20-21 to overcome this rejection. Applicants request that the amendments be approved and the rejection be removed.

35 U.S.C. §102

Claims 16 and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Luning et al., U.S. Patent 6,506,642, hereafter referred to as Luning. Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as recited in Claims 16 and 20-22 are not taught or suggested by Luning for the following rational.

Applicants respectfully direct the Examiner to amended Claim 16, which recites that an embodiment of the present invention is directed to (emphasis added):

A method for simultaneously manufacturing a semiconductor comprising a wide sidewall spacer and a narrow sidewall spacer comprising:

a) depositing a first layer over a first transistor comprising a gate stack, a drain side sidewall and a source side sidewall and over a second transistor comprising a gate stack, a source side sidewall and a drain side sidewall;

b) etching said first layer wherein a portion of said first layer remains on said source side sidewall and on said drain side sidewall of said first transistor and on said source side sidewall and on said drain side sidewall of said second transistor;

c) etching said first layer from said source side sidewall of said second transistor <u>while preserving said first layer on said drain sidewall of said second transistor</u>;

d) depositing a second layer over said first transistor and said second transistor; and

e) etching said second layer wherein a portion of said second layer remains on said first layer formed on said source side sidewall and on said drain side sidewall of said first transistor and wherein said second layer remains on said source side sidewall and on said drain side sidewall of said second transistor.

Independent Claim 16 has been amended to include the limitation "while preserving said first layer on said drain sidewall of said second transistor." This limitation is not taught or suggested by Luning. In fact, Luning <u>teaches away</u> from this limitation by teaching removal of the first layer on the drain sidewall. Figures 5 and 6 clearly show the first layer 44 is removed from the transistor 41. For this rational, Claims 16 and 20-22 are patentable over Luning. As such, allowance of Claims 16 and 20-22 is solicited.

35 U.S.C. §103

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Luning. The rejection is traversed for the following rational.

For the rational presented above, Luning fails to teach or suggest "while preserving said first layer on said drain sidewall of said second transistor," as claimed in independent Claim 16. Claim 23 depends on Claim 16 and recites further limitations. As such, Claim 23 is patentable over Luning and allowance of Claim 23 is solicited.

Claims 1-5 and 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai (U.S. Patent No. 6,352,891), hereafter referred to as Kasai, in view of Luning. Applicants have reviewed the cited references and assert that the embodiments of the present invention as recited in Claims 1-5 and 7-15 are patentable over Kasai in view of Luning for the following rational.

Applicants respectfully direct the Examiner to amended Claim 16, which recites that an embodiment of the present invention is directed to (emphasis added):

A method of manufacturing a semiconductor device comprising:

a) depositing a first layer over a periphery transistor comprising a gate stack, a drain side sidewall and a source side sidewall and over a

core transistor comprising a gate stack, a source side sidewall and a drain side sidewall;

b) etching said first layer wherein a portion of said first layer remains on said source side sidewall and on said drain side sidewall of said periphery transistor and on said source side sidewall and on said drain side sidewall of said core transistor;

c) etching said first layer from said source side sidewall of said core transistor while preserving said first layer on said drain side sidewall of said core transistor;

d) depositing a second layer over said periphery transistor and said core transistor; and

e) etching said second layer wherein a portion of said second layer remains on said first layer formed on said source side sidewall and on said drain side sidewall of said periphery transistor and wherein said second layer remains on said source side sidewall and on said drain side sidewall of said core transistor.

Independent Claim 1 has been amended to include the limitation "while preserving the first layer on the drain side sidewall of the core transistor," as claimed. This limitation is not taught or suggested by Luning. In fact, Luning teaches away from this limitation by teaching removal of the first layer on the drain sidewall. Figures 5 and 6 clearly show the first layer 44 removed from transistor 41.

Kasai fails to remedy the deficiencies of Luning. In fact, like Luning, Kasai teaches away from "while preserving the first layer on the drain side sidewall of the core transistor," as claimed, by teaching removal of the layer on the drain side of the transistor. Figure 9 clearly shows the first layer removed from the transistor on the peripheral side. The combination of Kasai and Luning fails to teach or suggest preserving the layer on the drain side, as claimed in

independent Claim 1. Independent Claim 9 teaches similar limitations of Claim 1. For this rational, the embodiments of the present invention, as taught in Claims 1-5 and 7-15, are patentable over Kasai in view of Luning.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai in view of Luning and yet further in view of Sun et al. (U.S. Patent No. 5,933,730), hereafter referred to as Sun. Applicants have reviewed the cited references and assert that the embodiments of the present invention as recited in Claim 6 are patentable over Kasai in view of Luning and yet further in view of Sun for the following rational.

As stated above, Kasai and Luning teach away from the claimed limitations of the present invention by teaching removal of the layer on the drain side. Sun fails to remedy the deficiencies of Kasai and Luning. Sun actually teaches away from the claimed limitations of the present invention by teaching that the layers are not etched from the sidewall of the transistor.

Figures 9j and 9k clearly show the first and second spacers remain on the sidewalls of the transistors. Sun may purport to teach a self-aligned source etch, however, Sun fails to teach or suggest "etching said first oxide layer from said source side sidewall of said core transistor while preserving said first layer on said drain side sidewall of said core transistor," as claimed. For this rational,

Claim 6 is patentable over Kasai in view of Luning and yet further in view of Sun. As such, allowance of Claim 6 is solicited.

CONCLUSION

In light of the above listed remarks, reconsideration of the amended Claims is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-23 overcome the rejections and objections of record and, therefore, allowance of Claims 1-23 is earnestly solicited.

Should the Examiner have a question regarding the instant response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,

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